

MULTI-CHIP ELECTRONIC PACKAGE AND COOLING SYSTEMRelated Applications

5 This application is related to co-pending U.S. Patent Application No. _____ filed _____ entitled "MULTIPLE CHIP STACK STRUCTURE AND COOLING SYSTEM"

Background of the InventionField of the Invention

10 The present invention relates to semiconductor processing technology and, in particular, concerns an electronic module comprised of a multi-chip electronic package having improved heat dissipation.

Description of the Related Art

15 Semiconductor manufacturers continually strive to increase the packaging density of integrated circuit chips, which has led to the development of high-density electronic packaging modules such as three-dimensional multi-chip structures. Multi-chip structures typically comprise a plurality of integrated circuit chips that are adhered together in a stack so as to reduce the amount of space that the chips occupy inside a system. Typically, each chip in the stack has a plurality of conductive input/output contacts that are exposed on at least one lateral surface of the chip. The exposed contacts provide conductive interconnection between the chips in the stack and external circuitry.

25 As a result of the increased device density of VLSI (Very-Large-Scale Integration) and ULSI (Ultra-Large-Scale Integration) integrated circuitry, wiring interconnective metallurgy between input/output terminals of stacked integrated circuit chips has become increasingly more complex. A higher packaging density likely requires an increase in the number of conductors, which likely reduces the space between adjacent conductors. Unfortunately, such dimensional reductions tend to 30 increase the capacitance between adjacent conductors, thereby possibly increasing signal propagation delays and signal cross-talk. The limitations brought about by

capacitive coupling between adjacent conductors has become a significant impediment to achieving higher wiring density.

The capacitive coupling effect is particularly apparent in high-density electronic packaging modules, such as three-dimensional multi-chip structures. In some multi-chip structures, the conductive leads on the integrated circuit chips are closely spaced, and adjacent leads may sometimes be separated by less than 1 micron. Consequently, reducing the distance between adjacent leads may adversely impact the functionality of the multi-chip structure due to an increase in the capacitive load between adjacent conductors. In addition, stacking the chips in close proximity to one another as required in multi-chip structures may also increase the capacitive coupling effect between conductors of adjacent chips.

Many integrated circuit chip designers have tried to address the problem of increased capacitive coupling between adjacent conductors by utilizing insulative materials that have lower dielectric constants than conventional dielectrics such as silicon-dioxide (SiO_2), which has a dielectric constant of about 4.5. In some cases, polymers, such as polyimides, which have a dielectric constant of about 2.8-3.5, have been used in place of SiO_2 . However, the polyimides provide limited improvement for the capacitive coupling problem and, therefore, do not provide a significant advantage in use.

Alternatively, interconnects incorporating an air bridge structure have also been developed and are described in prior art references such as U.S. Patent No. 5,891,797 to Farrar. Air bridge structures generally comprise suspended conductors that are surrounded by an air gap instead of the more conventional insulators. For example, U.S. Patent No. 5,324,683 to Fitch et al. describes the formation of an air bridge structure in an integrated circuit by removing all or a portion of the dielectric layer between conductors so that the conductors are surrounded and insulated by an air gap. Air has a dielectric constant of approximately 1.0, which is substantially less than the dielectric constants of conventionally used insulators such as SiO_2 or various polyimides. As such, the air-gap insulator provides some improvement for the capacitive coupling effect associated with the increased wiring density of integrated circuit chips.

Although air bridge structures permit an increase in the integrated circuit wiring density, the use of air bridges introduces some new problems such as the effective removal of heat from the air bridge structures. Generally, increasing the integrated circuit wiring density leads to a decrease in the cross-sectional area of the conductors.

5 As the cross-sectional area of an air bridge conductor decreases, the electrical resistance of the conductor increases, which results in an increase of the operating temperature of the conductors.

Excessive heat generation is particularly apparent in high-density multi-chip electronic packages, such as multi-chip modules or three-dimensional multi-chip structures. As the number of components in a multi-chip electronic package increases and the packaging density becomes more compact, the ability of heat to dissipate efficiently diminishes, which increases the risk of self-overheating and may reduce the reliable life of the semiconductor device. Moreover, integrated circuit and device functional characteristics may also depend on ambient temperature within the multi-chip electronic package. Therefore, as the ambient temperature of the package increases due to excessive heat generated by the conductors, hot spots within the multi-chip electronic package may form and adversely affect the performance of the integrated circuit.

Hence, from the foregoing, it will be appreciated that there is a need for an electronic module having higher wiring density combined with an efficient cooling system that effectively removes heat from the module. What is proposed herein is a densely packed electronic module having improved heat dissipation efficiency and a process of manufacturing the same.

Summary of the Invention

25 In one aspect, the preferred embodiments of the present invention provide an electronic packaging module comprising a plurality of integrated circuit chips stacked and secured together to form a chip stack wherein the chip stack has a first lateral face that is comprised of a first portion of each chip. The module further comprises an enclosure enclosing the chip stack. Preferably, the enclosure is configured to receive and enclose a thermally conductive fluid having a thermal conductivity greater than that of air at one atmosphere, wherein said thermally conductive fluid contacts the chip stack

and transfers heat away from the chips. In one embodiment, the thermally conductive fluid comprises a hydrogen and helium gas mixture. In another embodiment, the gas mixture is pressurized within the enclosure.

In another embodiment, at least one chip in the stack has a support frame that
5 extends from an upper surface of the chip substrate and along an outer perimeter of the substrate so as to define a spatial region containing interconnection wiring, including air bridge conductors. The support frame further comprises a plurality of openings that are configured to permit the thermally conductive fluid to flow therethrough and contact the interconnection wiring in the spatial region even though the chip is sandwiched in a
10 stack. Furthermore, in yet another embodiment, the support frame further comprises an upper portion that serves as a spacer separating the chip from adjacent chips. Advantageously, the thickness of the upper portion can be adjusted in accordance with the desired distance between adjacent chips and/or between rows of conductive contacts on adjacent chips.

15 In another aspect, the preferred embodiments provide an electronic packaging module comprising a plurality of integrated circuit chips stacked and secured together to form a chip stack that has four lateral faces with each lateral face comprising a portion of each chip. Furthermore, three exterior chips are mounted respectively to three of the lateral faces of the chip stack in a manner such that a surface of each exterior chip extends across at least a portion of each respective lateral face. The module also comprises a bonding substrate that is electrically connected, preferably via C4 connection, to conductive contacts formed on the fourth lateral face of the chip stack. Preferably, the conductive contacts are aligned to bond with the C4 structures on the substrate by precisely controlling the thickness of the spacer separating adjacent chips.
20 Furthermore, the module comprises an enclosure that encloses the chip stack, the exterior chips, and at least a portion of the bonding substrate. The enclosure also contains a thermally conductive fluid having a thermal conductivity greater than that of air and the fluid makes contact with at least some of the chips and transfers heat away from said chips.
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30 In yet another aspect, the preferred embodiments of the present invention provide an electronic packaging module that is comprised of a plurality of

semiconductor substrates stacked and secured together to form a multi-chip structure. Preferably, the multi-chip structure has a plurality of openings that are formed between two adjacent substrates in a manner so as to permit a fluid to circulate in a region between the substrates, thereby providing cooling for the multi-chip structure.

5 In yet another aspect, the preferred embodiments of the present invention provide a method of forming an electronic packaging module. The method comprises forming a support frame on an upper surface of a first semiconductor substrate. Preferably, the support frame extends from the upper surface of the substrate and defines a protected spatial region for interconnection wiring. Preferably, the support frame also comprises a plurality of openings on a lateral surface of the support frame so as to permit a thermally conductive fluid to enter said spatial region and remove heat from the air bridge conductors and other interconnection wiring formed in the spatial region. In one embodiment, a temporary support material is also formed on the upper surface of the substrate in a manner such that the temporary support material stabilizes and provides structure support for the air bridge conductors so as to permit the chip to be processed and handled without causing damage to the air bridges and other interconnection. The method further comprises assembling the first semiconductor substrate in a chip stack in a manner such that an upper surface of the support frame is positioned adjacent to a lower surface of a second semiconductor substrate. Preferably, the temporary support material is removed from the substrate after the chip is completely assembled in the chip stack. The method further comprises enclosing the chip stack inside an enclosure and introducing a thermally conductive fluid to the enclosure. The thermally conductive fluid has a thermal conductivity greater than that of air and the conductive fluid travels through the opening in the support frame and contacts the air bridge conductors formed in the spatial region and removes heat therefrom. These and other advantages of the present invention will become more fully apparent from the following description taken in conjunction with the accompanying drawings.

Figure 1 is a partial schematic illustration of one embodiment of an integrated circuit chip that can be incorporated into a multi-chip electronic module of the preferred embodiment;

5 Figure 2 is a partial schematic cross-sectional view of a chip stack incorporating the chip shown in Figure 1;

Figure 3 is a schematic perspective view of the chip stack of Figure 2;

Figure 4 is a multi-chip structure incorporating the chip stack of Figure 3;

Figure 5 is a schematic illustration of a high-density electronic packaging module of the preferred embodiment incorporating the multi-chip structure of Figure 4.

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Detailed Description of the Preferred Embodiment

References will now be made to the drawings wherein like numerals refer to like parts throughout. Figure 1 is a partial schematic illustration of one embodiment of an integrated circuit chip 100 that can be incorporated into a multi-chip electronic module of the preferred embodiment. As shown in Figure 1, the chip 100 comprises a substrate 102, such as a silicon substrate, that carries a variety of integrated circuitry and devices, such as capacitors, resistors, transistors, memory cells, and logic gates, that are formed using conventional semiconductor manufacturing processes. As also shown in Figure 1, the chip 100 further comprises a support frame 104, a plurality of air bridge structures 106, and a temporary support material 107 that are each formed on an upper surface 108 filling the remaining space of the substrate 102 using methods known in the art or, more preferably, in accordance with methods described in Applicant's co-pending U.S. Patent Application entitled "PACKAGING OF ELECTRONIC CHIPS WITH AIR-BRIDGE STRUCTURES", Attorney Docket No. 303.603US1, which is incorporated by reference herein in its entirety.

As Figure 1 illustrates, the support frame 104 is substantially rigid and extends from the upper surface 108 of the substrate 102 in a manner so as to protect the air bridge structures 106 and other interconnection wiring from being damaged by the weight of adjacent chips when the chip 100 is placed in a multi-chip stack and by handling during assembly of the stack. In one embodiment, the support frame 104 preferably extends along an outer perimeter 110 of the substrate 102 in a manner so as

enclose the interconnection wiring formed on the upper surface 108 of the substrate 102. In another embodiment, the support frame 104 further includes a plurality of reinforcement ribs 112 that extend across the length and width of the substrate 102 to provide additional mechanical support and protection for the chip 100 and its interconnection wiring when the chip 100 is placed in a stack with other chips.

As Figure 1 further illustrates, the support frame 104 defines a protected spatial region 114 extending above the upper surface 108 of the substrate 102. The spatial region 114 preferably comprises wiring levels 116 that are suitable for formation of air bridges 106 and other interconnection wiring. A wiring level is herein defined as a planar section above and substantially parallel to the upper surface of the substrate which contains air bridges and other conductors that extend in the same general plane. It can be appreciated that the chip 100 may comprise any number of wiring levels and is not limited to the number of wiring levels shown in Figure 1.

Furthermore, the support frame 104 preferably has an upper portion 118 extending above the uppermost wiring level. The upper portion 118 preferably serves as a spacer separating the chip 100 from subsequently mounted adjacent chips. As will be described in greater detail below, the thickness of the upper portion 118 can be dimensioned in accordance with the particular spacing desired between adjacent chips. In one embodiment, the upper portion 118 is dimensioned so that the chip 100 when stacked in a multi-chip structure will be in proper alignment with conductive contacts, such as C4 contacts, positioned on chips that are subsequently mounted to the lateral faces of the multi-chip structure. Advantageously, the upper portion 118 of the support frame 104 may replace the conventional insulator spacer material that is typically interposed between adjacent chips in a chip stack. Because the upper portion 118 of the support frame 104 is substantially rigid and has a uniform thickness, it allows for more precise control and tuning of the distance separating adjacent chips in a chip stack.

Additionally, as shown in Figure 1, the support frame 104 further comprises a plurality of openings 120 that are formed on a lateral surface 122 of the frame 104 using methods known in the art. As will be described in greater detail below, the openings 120 allow a thermally conductive medium, such as air, gas, or even liquid, to enter the spatial region 114 containing the air bridge structures 106 and circulate therethrough,

thus removing heat generated from the conductors in the spatial region 114. Advantageously, the openings 120 permit a thermally conductive medium to circulate freely in and out of the spatial region 114 enclosed by the support frame 104 even when the chip 100 is placed in a stack with other chips. The openings 120 can be positioned at various locations on the support frame 104 and can take on a variety of different sizes and shapes without departing from the spirit of the invention.

In one embodiment, the support frame 104 is fabricated by depositing a layer of metal on the upper surface 108 of the substrate 102 using chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), physical vapor deposition (PVD) techniques, electro-plating, electroless plating, sputtering, and/or electroforming. The metal layer is subsequently patterned and etched to define the configuration of the frame 104. In another embodiment, the support frame 104 and interconnection wiring for each wiring level are formed in the same process set using methods disclosed in Applicant's co-pending U.S. Patent Application, entitled "MICROELECTRONIC DEVICE PACKAGING WITH CONDUCTOR ELEMENT", which is incorporated by reference herein in its entirety. The support frame 104 can be made of a conductive material such as copper. Alternatively, the support frame 104 may comprise copper and an organic and/or inorganic insulating insert material. The insulating insert material is preferably incorporated in the reinforcement ribs 112 adjacent to where air bridge conductors are likely to extend through the ribs. In other embodiments, the support frame 104 may comprise an insulator made of organic and/or inorganic materials.

As Figure 1 further shows, the temporary support material 107 formed on the upper surface 108 of the substrate 102 fills substantially the entire spatial region 114 comprising the interconnection wiring so as to stabilize and provide temporary structural support for the air bridges 106 and other circuitry therein. The temporary support material 107 permits the chip 100 to be processed and handled without causing damage to the air bridge conductors 106 or support frame 104 during subsequent process steps. The temporary support material 107 may be formed on the upper surface 108 of the substrate 102 using generally known chemical deposition processes. Preferably, the temporary support material 107 is polished back to a thickness that just exposes an upper surface 124 of the support frame 104 as shown in Figure 1, which

provides the chip with a leveled surface 124 for mounting as well as electrical bonding. The upper surface 124 of the support frame 104 and additional metal ledges (not shown) formed on the outside of the support frame 104 can be used to facilitate electrical detection of the end points during the process of removing the support material 107.

5 As described above, the temporary support material 107 stabilizes the air bridge structures 106 and the support frame 104 formed on the substrate 102, thus allowing the chip 100 to be handled and processed without being damaged. As such, the support material 107 preferably is not removed until the chip 100 has been assembled into a multi-chip stack. In one embodiment, the temporary support material 107 may 10 comprise carbon or other materials that can be oxidized or otherwise chemically removed with relative ease. In another embodiment, the temporary support material 107 may comprise a polymer such as high temperature polyimide, a photoresist, parylene such as parylene C or any combinations thereof.

Furthermore, as shown in Figure 1, the air bridge structures 106 are formed 15 above the upper surface 108 of the substrate 102 to electrically interconnect a first and a second exposed contact 128a, 128b extending from the upper surface of the substrate 102. Each air bridge structure 106 generally comprises a conductor 126 that is suspended by the two or more conductive contacts 128a, 128b. As described above, the conductors 126 are stabilized and supported by the temporary support material 107, but 20 will become suspended in air once the temporary support material 107 is removed. The air bridges 106 can be formed using methods known in the art such as damascene or dual damascene processes. Furthermore, Applicant also discloses a method of forming air bridge interconnects in U.S. Patent No. 5,891,797 to Farrar entitled "METHOD OF FORMING A SUPPORT STRUCTURE FOR AIR BRIDGE WIRING OF AN 25 INTEGRATED CIRCUIT," which is hereby incorporated by reference in its entirety. In one embodiment, the air bridge structures 126 may be fabricated using conductive materials, such as aluminum, copper, gold, silver, platinum, polysilicon, and amorphous silicon. In addition, methods for depositing conductive air bridge interconnects may include deposition processes, such as chemical vapor deposition (CVD), and physical vapor deposition (PVD), sputtering and electron beam evaporation or various liquid 30 deposition techniques.

As Figure 1 also shows, the air bridge conductors 126 may be further supported by a plurality of intermediate posts 130 that are formed on the upper surface 108 of the substrate 102. Once the temporary support material 107 is removed from underneath the conductors 126, the posts 130 are preferably used to support the longer air bridge conductors as the longer conductors may sag in the center and touch a neighboring air bridge interconnect, which may cause an electrical short therebetween. To reduce the occurrence of sagging, some longer air bridge interconnects may require more than one intermediate posts along the length of the bridge. The posts 130 may be formed using methods generally known in the art or those described in U.S. Patent No. 5,891,797 to Farrar, or, more preferably, methods described in Applicant's co-pending Application entitled "PACKAGING OF ELECTRONIC CHIPS WITH AIR-BRIDGE STRUCTURES", Attorney Docket No. 303.603US1. In one embodiment, the posts 130 are comprised of an insulating material such as SiO₂ or a polymer such as polyimide. In another embodiment, the posts 130 are comprised of the same material as the air bridge conductors 124, however insulator inserts are interposed between the posts and the substrate.

Figure 2 provides a partial schematic cross-sectional view of a chip stack 132 incorporating the chip 100 described and shown in Figure 1. The chip stack 132 comprises a plurality of chips 100 that are stacked together in a manner such that the upper surface 124 of the support frame 104 of one chip is positioned adjacent to a lower surface 134 of the substrate 102 of another chip. The chips 100 may be bonded to each other using C4 contacts and/or adhesives as described in the Applicant's co-pending U.S. Patent Application entitled "A THREE DIMENSIONAL MULTI-CHIP STRUCTURE AND METHOD OF MAKING THE SAME", Attorney Docket Number MICRON.184A, which is incorporated by reference herein its entirety.

Furthermore, as described above, the thickness of the upper portion 118 of the support frame 104 can be fine tuned in accordance with the distance desired between chips 100. In one embodiment, the temporary support material 107 is removed once the chip stack 132 is assembled. However, in embodiments that involve mounting additional exterior chips to the lateral faces of the chip stack, the temporary support material 107 is preferably removed after the exterior chips are mounted. The temporary

support material 107 is preferably chemically removed in a manner that does not damage the devices and circuitry formed on the chips. In one embodiment, the temporary material 107 is oxidized in an environment containing molecular oxygen or ozone or an oxygen plasma. In an oxidation process utilizing molecular oxygen, the
5 process time, temperature and pressure can be increased to effectively remove substantially all carbon-based materials. In a plasma oxidation process, the lower pressures utilized are likely to facilitate complete removal of all organics. As such, it is desirable to use readily oxidized polymeric materials or carbon as the temporary support and/or spacer materials.

10 As Figure 2 further shows, a plurality of conductive leads 136 extend from interconnects on the uppermost wiring level, through the support frame 104, and toward an outer edge 138 of the chip 100. Preferably, the leads 136 extend past the chip edge 138 and serve as electrical contact points with external circuitry. In cases where the support frame 104 is made of a conductive material, the leads 136 are preferably routed
15 through an insulator insert 140 formed on the support frame 104 as shown in Figure 2.

Figure 3 provides a schematic perspective view of the chip stack 132. As shown in Figure 3, the chip stack 132 comprises a plurality of lateral faces 142a, b, c, d and an upper and a lower face 144a, b. Preferably, each lateral face of the stack 132 is comprised of a side surface of each chip 100 and the upper and lower faces of the stack 20 132 comprise the respective outer substrate surfaces of the chips located on the ends of the stack. Figure 3 also shows a plurality of electrical contacts 146 are formed the lateral faces 142a, b, c, d of the chips stack 132. These electrical contacts 146 are preferably interconnected to the conductive leads that extend from the upper wiring level of each chip 100. In one embodiment, the chips 100 in the stack 132 are memory
25 chips. In another embodiment, only a portion of the chips in the chip stack 132 incorporate the air bridge structures and the support frames as described above while the remaining chips utilize conventional circuitry and spacer material between chips so as to improve the overall structural integrity and ruggedness of the chip stack 102.

With reference to Figure 4, a plurality of exterior chips 150a-e are mounted to
30 the lateral, upper and lower faces of the chip stack 132 to form a multi-chip module 148. The exterior chips may comprise integrated circuit chips of an entire system including

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processor chips, memory chips, logic chips, and A/D converter chips that may not be included in most conventional integrated circuit chips due to overheating and chip interconnection problems. The exterior chips can be mounted and interconnected to the chip stack using C4 connections, modified C4 connections and other methods disclosed in Applicant's co-pending U.S. Patent Applications, entitled "A THREE DIMENSIONAL MULTI-CHIP STRUCTURE AND METHOD OF MAKING THE SAME", Attorney Docket Number MICRON.184A and "ANGLED INTERCONNECT", Attorney Docket Number MICRON.245A, which are hereby incorporated by reference in its entirety. As described above, in one embodiment, the distance between rows of conductive interconnects on adjacent chips are precisely fixed by the upper portions of the support frame on each chip so that the interconnects may be aligned with the C4 structures formed on the exterior chips. Figure 4 further shows that the multi-chip structure 148 is electrically interconnected to external circuitry formed on a bonding substrate 152. In one embodiment, the fourth lateral face 142d of the chip stack 132 is preferably bonded to an upper surface 154 of the substrate 152 in a manner such that electrical contacts (not shown) on the fourth lateral face 142d is interconnected with circuitry formed on the upper surface 154 of the bonding substrate 152. Generally known techniques such as C4 connections and flip-chip bonding may be used to establish electrical interconnection. In another embodiment, a heat sink may be attached to the stack 132 prior to bonding to the substrate 152.

Figure 5 provides a schematic illustration of a high-density electronic packaging module 200 of the preferred embodiment in which the multi-chip structure 148 is enclosed in an enclosure 202 filled with a thermally conductive medium 204. As shown in Figure 5, the enclosure 202 comprises a plurality of walls 206 defining an interior space 208 that is sufficiently large to contain the multi-chip structure 148 and still retain sufficient free space to permit the thermally conductive medium 204 to circulate around the multi-chip structure 148. Preferably, the thermally conductive medium 204 acts as a heat sink by contacting the air bridges and other circuitry and devices in the multi-chip structure and transferring heat generated therefrom to the thermally conductive medium. Although the chips 100 are stacked together, the thermally conductive medium 204 is able to circulate to and from the air bridge structures and other conductors within the

stack by traveling through the openings formed on the lateral surfaces of the support frames in each chip.

In one embodiment, the enclosure 202 is placed over the multi-chip structure 148 and attached to the upper surface 154 of the bonding substrate 152. Preferably, the 5 enclosure is hermetically sealed to the bonding substrate so as to isolate the structure 148 from the external environment and to retain the thermally conductive medium 204 inside the enclosure. The enclosure 402 may be formed of an insulator material or a conductive material, such as glass or metal, in a manner known in the art. Preferably, the enclosure 402 is comprised of a copper alloy having a high thermal conductivity and 10 sufficiently rigid to support a pressurized fluid. Moreover, the enclosure 402 is preferably comprised of a material that inhibits diffusivity of the thermally conductive medium 204.

In one embodiment, the thermally conductive medium 204 comprises a thermally conductive gas having a thermal conductivity greater than that of air. 15 Preferably, the gas comprises pure hydrogen, helium, or a hydrogen-helium gaseous mixture. There are a number of advantages in selecting a hydrogen-helium gaseous mixture as the thermally conductive medium 204. First, the thermal conductivities of hydrogen and helium are similar to each other and much higher than those of most other gases. Second, the permeability or diffusivity of molecular hydrogen through some 20 metals, glasses, and other enclosures is significantly smaller than that of helium, and hence is less prone to diffuse out of an enclosure over time. However, the use of pure hydrogen gas may raise some safety concerns under certain operating conditions. Thus, a hydrogen/helium gas mixture provides a gas mixture that has high thermal conductivity, relatively low diffusivity, and yet does not raise any substantial safety 25 concerns. In one embodiment, the gas mixture comprises about 10% hydrogen and 90% helium. Other embodiments may comprise various other ratios of hydrogen to helium.

Furthermore, the thermally conductive medium 204 may be pressurized so as to increase the density of the gas mixture that is enclosed by the enclosure 202. In one embodiment, the pressure of the thermally conductive fluid is maintained between a 30 range of 5 MPa and 50 MPa. Advantageously, the thermal conductivities of hydrogen and helium are approximately proportional to their pressures and the thermal

conductivity of a pressurized mixture of hydrogen and helium is remarkably high. For example, a hydrogen/helium gas mixtures at pressures of about 5 to 50 MPa yield thermal conductivities of about 1.6×10^{-3} to 1.6×10^{-2} cal-cm/sec, respectively. When compared with a thermal conductivity value of about 2.3×10^{-2} for fused silicon and about 5.7×10^{-5} for air at atmospheric pressure, a hydrogen/helium mixture at 50 MPa pressure is almost 300 hundred times that of air at atmospheric pressure. However, it can be appreciated that the optimum gas compositions and pressures will vary with the particular application being used. For example, in relatively larger volume packages, less helium-rich mixtures may suffice since loss of helium via out-diffusion through the enclosure may be insignificant. In small electronic packages, the use of pure hydrogen may be preferred since the thermal conductivity may be higher, out-diffusion may be negligible, and safety concerns may be relatively insignificant. It can also be appreciated that the thermally conductive medium 204 is not limited to any gaseous mixture and may comprise any type of thermally conductive fluid, including liquids.

Although the multi-chip structure 148 of the preferred embodiment comprises air bridge structures that utilize air gap as an insulator, the electronic packaging module 200 is not limited to multi-chip structures that incorporate air insulators. In fact, the packaging module 200 may incorporate multi-chip structures that utilize various approaches for insulating the metallurgical interconnection layers including low thermal conductivity spacer layers, such as low density polymeric foams, and/or insulator structures, such as silicon dioxide films and/or various hybrid insulating approaches. Implementation of the disclosed embodiments may be compatible with flip-chip bonding of the entire assembly to a ceramic substrate or other substrate. Furthermore, the enclosure 202 may be cooled using generally known cooling techniques, such as heat pipes, liquid coolants, external fins, and/or convective cooling fans.

Advantageously, the unique spacing configuration of the multi-chip structure 148 permits efficient cooling by utilizing a pressurized, thermally conductive medium as a heat sink. The hermetically sealed enclosure permits efficient, pressurized cooling of the multi-chip structures, which may increase the reliability of the chip structures by reducing the occurrence of thermal breakdown associated with the self-overheating of

integrated circuit components. Furthermore, increasing system reliability may reduce the incidence of system malfunctions.

As discussed above, densely packed integrated circuit chips such as those in a multi-chip structure tend to produce an increased amount of heat during normal operation. Therefore, an efficient system of cooling the chip by transferring a substantially amount of heat away from the chip improves the performance and reliability of the chip by reducing self-overheating. Advantageously, the electronic packaging module of the preferred embodiment provides a chip stack having open spaces created between adjacent chip substrates to allow a thermally conductive gas mixture to readily permeate the spaces and reach the air bridge conductors and other circuitry therein, which substantially reduces thermal hot spots within the multi-chip electronic package.

Although the foregoing description of the various embodiments of the invention have shown, described, and pointed out the fundamental novel features of the present invention, it will be understood that various omissions, substitutions, and changes in the form of the detail of the apparatus as illustrated as well as the uses thereof, may be made by those skilled in the art, without departing from the scope of the present invention. Consequently, the scope of the present invention should not be limited to the foregoing discussions, but should be defined by the appended claims.